AMENDMENTS TO THE CLAIMS

Claims 1-31 were pending in the application. Claim 1 is an independent claim and claims 2-24 depend there from. Claim 25 is an independent claim and claims 26-31 depend there from. Claims 25-31 are currently withdrawn.

Listing of Claims

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Previously Presented) A system that enhances the performance of a cochlear implant using a preprocessor, the system comprising:

at least one signal input device;

a first processor coupled to said at least one signal input device for performing signal processing on signals received from said at least one signal input device, wherein said first processor comprises at least one automatic-switching mechanism configured to at least one of:

switch between modes of said at least one signal input device,

switch between said at least one signal input device, and

switch between a plurality of listening programs; and

a second processor that processes and encodes the signal in cochlear implants.

2. (Original) The system according to claim 1 wherein the at least one signal input device is one of microphones(s), direct audio input, telecoil, and other forms of analog or digital signals inlet.

3. (Previously Presented) The system according to claim 1 wherein the first processor comprises at least one of algorithms stored in a memory or chips used in hearing aids, hearing protectors, and other audio devices.

4. (Previously Presented) The system according to claim 1 wherein algorithms associated with the first processor are implemented in the same chip and case as algorithms associated with the second processor.

5. (Original) The system according to claim 1 wherein the first processor and at least one signal input device are housed in a first case.

6. (Original) The system according to claim 5 wherein the second processor and at least one signal input device are housed in a second case.

7. (Original) The system according to claim 6 wherein an output of the first processor is fed into the second processor.

8. (Original) The system according to claim 6 wherein the system further comprises:

a wireless transmitter connected to the first processor; and

a wireless receiver connected to the second processor, wherein an output of the first processor is wirelessly transmitted via the wireless transmitter to an input of the second processor via the wireless receiver.

9. (Original) The system according to claim 1 wherein the system further comprises a signal input device housed in a first case.

10. (Original) The system according to claim 9 wherein the first processor is housed in a first case.

11. (Original) The system according to claim 9 wherein the second processor is housed in the first case.

12. (Original) The system according to claim 9 wherein the system further comprises a circuit that provides compatibility matching between the first processor and the second processor.

13. (Original) The system according to claim 1 wherein the system further comprises signal input devices housed in a first and second case.

14. (Original) The system according to claim 13 wherein the first processor is housed in the first case.

15. (Original) The system according to claim 14 wherein the second processor is housed in the second case.

16. (Original) The system according to claim 13 wherein the second processor receives a processed signal from the first processor via the signal input device in the second case.

17. (Original) The system according to claim 1 wherein the system further comprises a signal input device housed in a first case.

18. (Original) The system according to claim 17 wherein the first processor and the second processor are housed in a second case.

19. (Original) The system according to claim 9 wherein the system further comprises a circuit that provides compatibility matching between the first processor and the second processor.

20. (Previously Presented) The system according to claim 1 wherein the first processor comprises at least one of:

at least one signal processing stage;

at least one signal processing algorithm stored in a memory; and

at least one component.

21. (Original) The system according to claim 20 wherein the second processor utilizes at least a portion of the first processor.

22. (Original) The system according to claim 21 wherein the first processor contains at least one signal feeding point and at least one signal extraction point to which connection can be made to feed signals into and extract signal from the system.

23. (Previously Presented) The system according to claim 1 wherein the second processor comprises multiple signal processing stages, wherein the first processor is connected between the multiple signal processing stages of the second processor.

24. (Original) The system according to claim 1 wherein the second processor is an amplification device.

25-31. (Withdrawn)